

Lightweight and Secure PUF Key Storage Using Limits of Machine Learning

VERAYO™



Meng-Day (Mandel) Yu¹, David M'Raihi¹, Richard Sowell¹, Srinivas Devadas²

¹Verayo, Inc., San Jose, CA, USA

²MIT, Cambridge, MA, USA

Agenda

Physical Unclonable Function (PUF) Overview

PUF Noise Profile

- Response size, temperature, voltage

Deriving Stable PUF Bits

- Traditional: Large block ECC, Two-stage ECC
- Lightweight: Stable bits w/o complex ECC

Security Framework

- *“Use what cannot be learned about the system”*

Conclusions

PUF Overview

Physical Unclonable Functions (PUF)



\neq

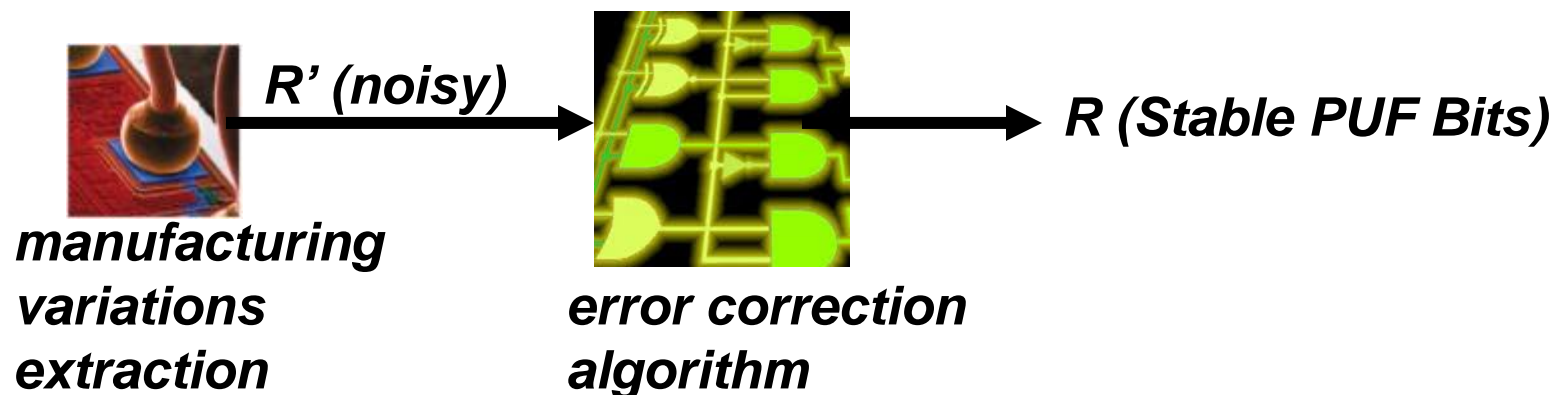


Tiny electronic circuits extract silicon *manufacturing variations*

Unique characteristics = “silicon biometrics”

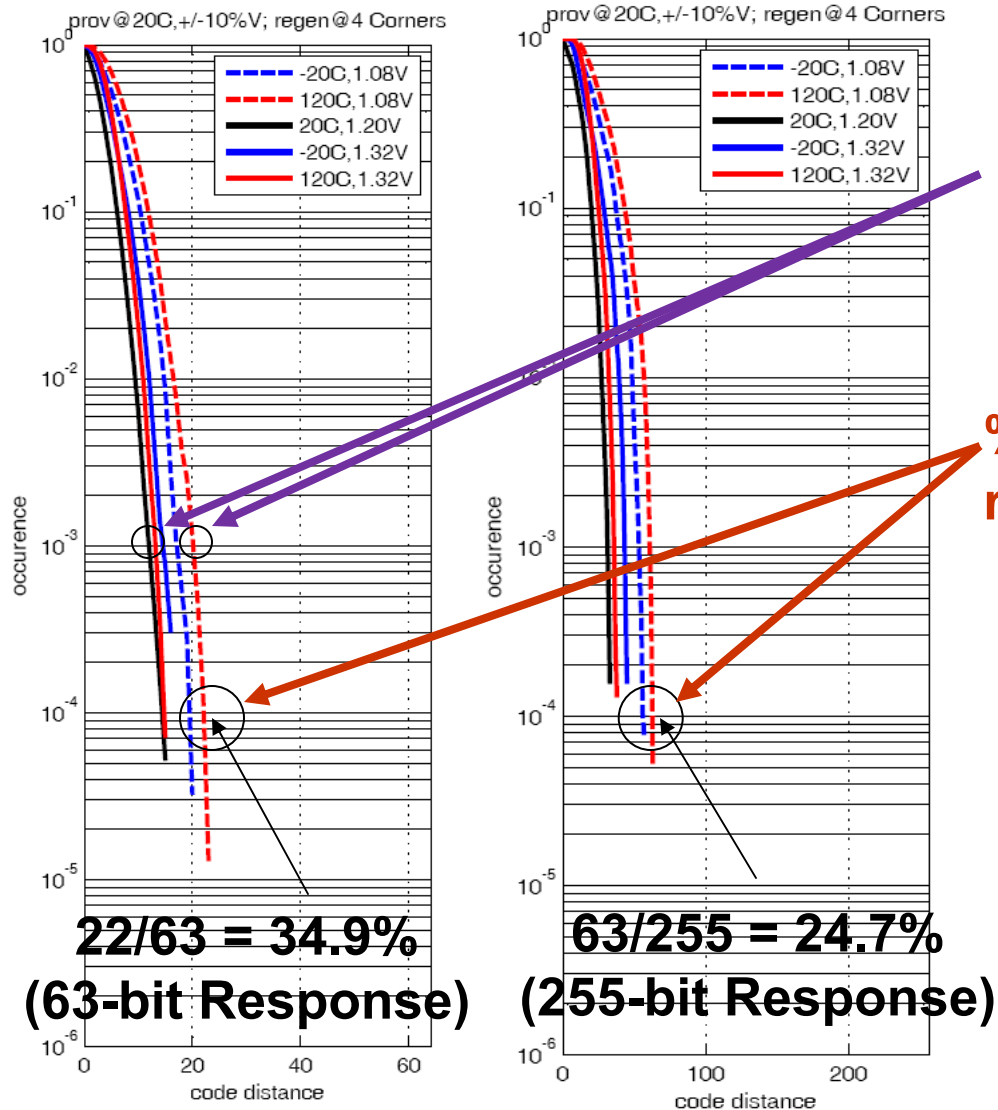
PUF responses are “noisy”

To generate Stable PUF Bits: add error correction algorithm



PUF Noise Profile

PUF Noise Profile



Unstable bits ↑ with $\Delta V, \Delta T$
 • Noise ↑ ~1.5x to ~2x

% of unstable bits ↓ with larger response size
 • BCH error correction limit = 25%
 • Use larger response size to correct noisier PUF

Deriving Stable PUF Bits

Methods to Derive Stable Bits

Large Block ECC

- Single stage error correction
 - BCH(255,63,t=30) [Suh-MIT2005]
 - BCH(255,13,t=59) [AMSSW-IEEE_S&P2011]

Two-stage ECC

- Quadratic reduction in complexity
 - Repetition(11,1,t=5) + Golay(24,13,t=3) [BGSST-CHES2008]
 - Repetition(11,1,t=5) + RM(16,5,t=3) [BGSST-CHES2008]
 - Repetition_{SoftDecision}(3,1,t=1) + RM_{SoftDecision}(64,22,t=7) [MTV-CHES2009]
 - IBS + BCH(63,30,t=6) [YD-IEEE_D&T2010]

Lightweight (no complex ECC)

- Use “Index Based Syndrome” (IBS) w/o BCH
- Additional complexity reduction (75%)
- Add retry, simple coding to improve reliability

Index-Based Syndrome (IBS) Coding

From [YD-IEEE_D&T2010]

Use a group of PUF output values to store a bit sequence

Simple case: a sequence of 1 bit

- Encoder:
 - If $\underline{B} = 1$, $\underline{S} = \text{index of } f_1(\underline{R}_0 = r_0, \dots, \underline{R}_{q-1} = r_{q-1})$
 - If $\underline{B} = 0$, $\underline{S} = \text{index of } f_0(\underline{R}_0 = r_0, \dots, \underline{R}_{q-1} = r_{q-1})$

Let $f_1 = \text{max function}$, $f_0 = \text{min function}$
 $\underline{B} = \text{bit to store}$, $\underline{S} = \text{Syndrome Word}$

- Decoder:
 - $\underline{B}' = \text{sign_of } (\underline{R}_s)$

Advantages:

- Trivially simple encoder and decoder
- High coding gain -> reduction in ECC complexity
- Provably secure (more later)

Size Comparisons (Xilinx Virtex-5 LX50)

Lightweight (IBS)	2-stage ECC (IBS + BCH63)	Large Block (BCH255)
69 registers	471 registers	6400 registers (est. using 16x)
~1.2% SLICE count (99/7200)	~5% SLICE count (393/7200)	~65% SLICE count

- Includes decoder + encoder
- Does not include APB interface, I/O buffering
- Even smaller if test logic, configurability removed



Decoder Core Comparisons (Xilinx Spartan 3E-500)

Retargeted implementation for Spartan 3E (w/o optimizations) for comparison

Use best results from [MTV-CHES2009], [BGSST-CHES2008]

Goal: 128-bit key

	Current Work		[MTV-CHES2009]	[BGSST-CHES2008] PUF-Optimized	[BGSST-CHES2008] Decoder-Optimized
Area	116 SLICES (no μ code required)		164 SLICES (μ code ROM required)	580 SLICES (μ code ROM required)	110 SLICES (μ code ROM required)
Dec Cycles	~16640 cycles (@ 100Mhz+)		~10298 cycles (@ 50.2Mhz)	>= 24024 cycles (@ 151.5Mhz)	>= 29925 cycles (@ 175.4Mhz)
Helper Data	780 bit		13952 bit	3824 bit	6288 bit
PUF Size	1280 OSC* (Security-Optimized)	256 OSC* (PUF-Optimized)	1536 bit SRAM**	3696 bit SRAM**	6160 bit SRAM**
Stability	-55°C to 125°C, V_{nom} +/- 10%, WC VT Corners, Aging		PUF noise model does not account for V,T.	PUF noise model accounts for -20°C to 80°C [GSST-CHES2007]. No voltage.	
Security	Insufficient equations to learn system (no i.i.d assumption)	Use unlearnable part of system (no i.i.d. assumption)	Soft decision information is information-theoretically secure (i.i.d. assumption)	No explicit security argument to account for leaks associated w/ heavy repetition coding	

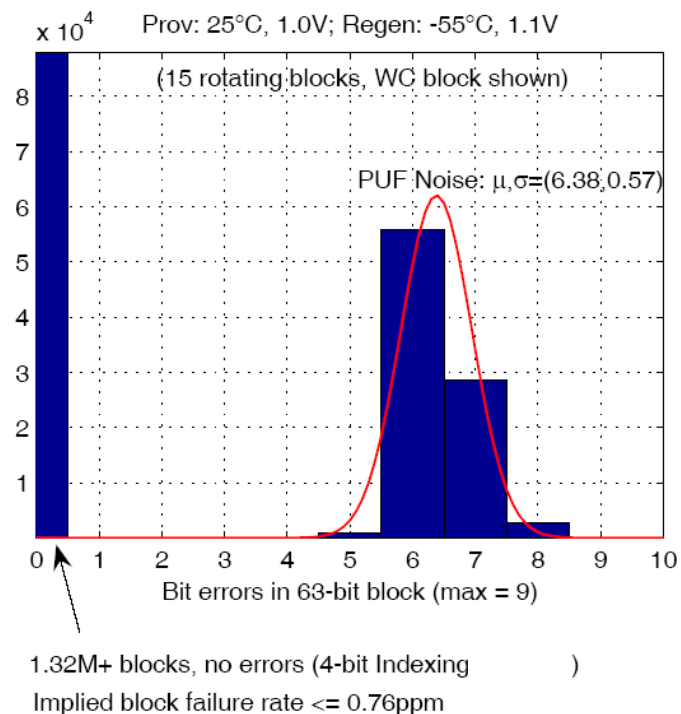
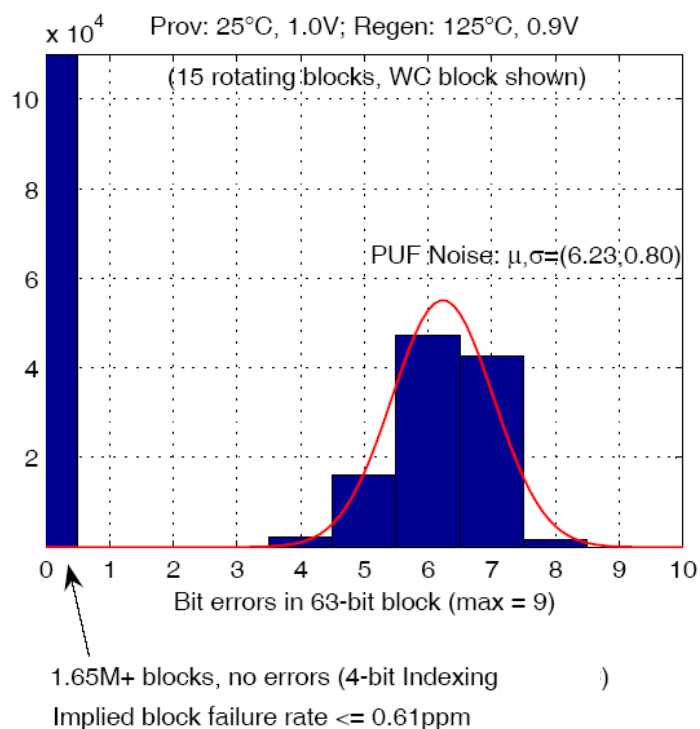
* 5 inversions per OSC (~3 NAND2 equivalent gate, 1st order est.) ** 6T cell per bit (~3 NAND2 equivalent gate)

WC Voltage / Temperature Corners

Empirical PUF data from Xilinx Virtex-5 FPGAs

Error Free Performance using 4-bit Index

- 1M+ blocks, implied failure rate < 1 ppm
- SS Corner 125°C, 0.9V
- FF Corner -55°C, 1.1V

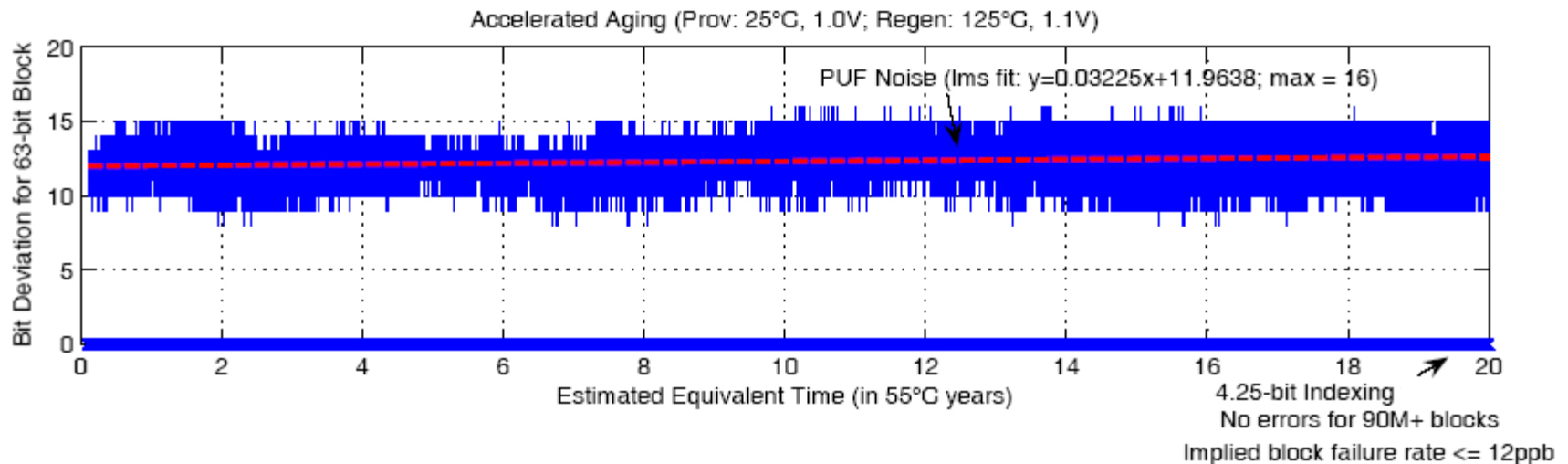


Accelerated Aging

~90M+ blocks, error free performance, 4.25 bit Index

- Implied error rate ≤ 12 parts per *billion* (ppb)
- Accelerated age: 20+ yrs @ 55°C
- Provisioning: 25°C, 1.0V; Regeneration: 125°C, 1.10V

Aging deteriorates silicon, increasing Indexing requirement by $\frac{1}{4}$ bit

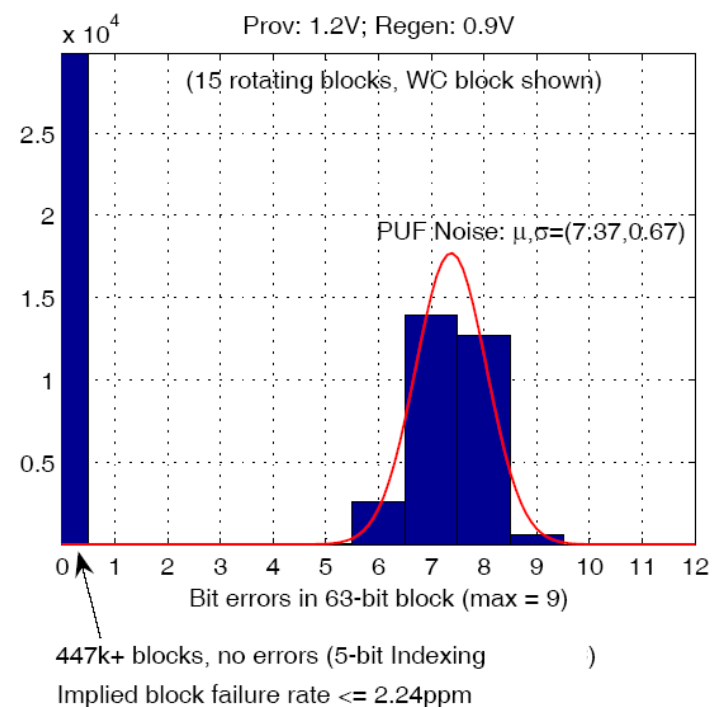
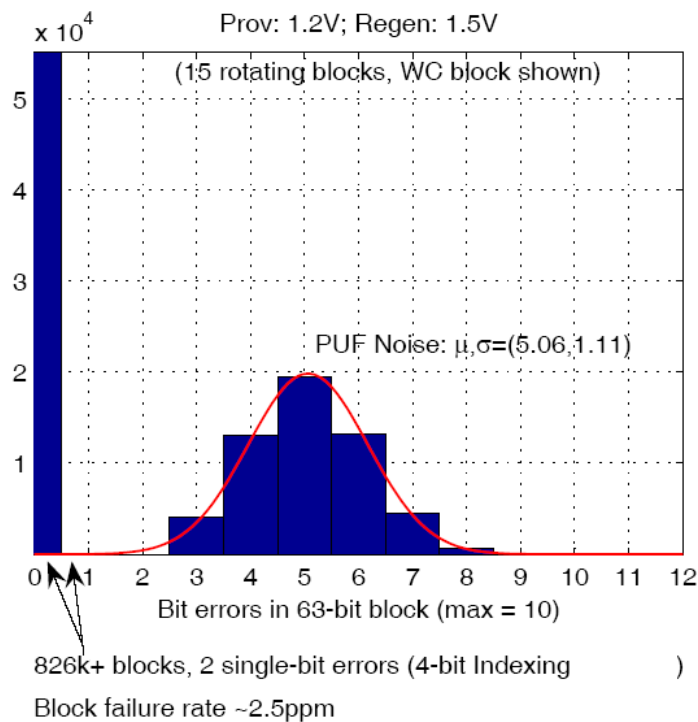


Voltage Testing, ASIC

PUF + Indexing Algorithm in .13 μ m silicon

- 4 to 5 bit Index for reliable (ppm level or better) operation

Results consistent with FPGA



Security Framework

Security Dependencies of Prior Work (1)

Recall: [BGSST-CHES2008]

- No explicit security argument for use of Repetition[11,1,t=5] code
- Heavy repetition coding highly sensitive to PUF bias:

$$\text{Bits leaked per repetition-coded bit} = \frac{|PUFbias - 0.5|}{\left\lfloor \frac{repetition}{2} \right\rfloor - 0.5}$$

[YD-IEEE_D&T2010]

1. if PUF bias = .55, all bits leaked!
2. if PUF bias = .505, 1 bit leaked out of every 9 bits repetition-coded
... this is true even if PUF output bits are assumed to be i.i.d.

Current work avoids heavy repetition coding

Security Dependencies of Prior Work (2)

[MTV-CHES2009] and [YD-IEEE_D&T2010] both use proofs that require i.i.d. PUF output assumption (implicitly or explicitly)

Questions:

- Memory PUF: Are there correlations based on memory word columns?
- Arbiter PUF / OSC PUF: Are there correlations with reuse of delay elements?

Can we remove i.i.d. assumption?

Unconditional Security

Recall:

- Shannon Entropy: $H(\underline{X}) = - \sum p(x) \log_2 p(x)$
- Mutual Information: $I(\underline{Y}; \underline{X}) = H(\underline{Y}) - H(\underline{Y} | \underline{X})$

Unconditional security (perfect secrecy) [Shannon, 1949]

- Ciphertext share no information with the Key
- Secure against a *computationally-unbounded* adversary
- **Strongest form of security**
- Information shared between Ciphertext and Key:
 - $I(\underline{CT}^{\text{alg}}; \underline{Key}) = H(\underline{Key}) - H(\underline{Key} | \underline{CT}^{\text{alg}})$

We adapt this unconditional security measure to develop a syndrome leakage metric...

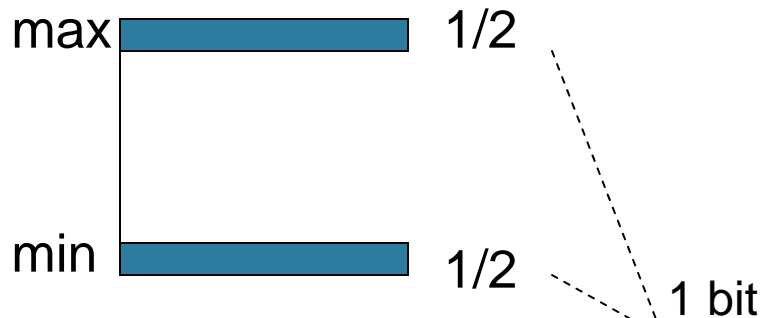
Leaked Bits (LB)

What is the information shared between a Syndrome Word and a perfect model of the PUF?

- Code offset [Dodis, 2004], 3x repetition coding
 - $\text{LB}(\underline{S}^{3x}) \equiv I(\underline{S}^{3x}; \underline{M}^p) = H(\underline{S}^{3x}) - H(\underline{S}^{3x} | \underline{M}^p) = 3 - 1 = 2 \text{ bits}$
- Index-Based Syndrome (IBS) Coding [Yu, 2010], 3-bit index
 - $\text{LB}(\underline{S}^{3i}) \equiv I(\underline{S}^{3i}; \underline{M}^p) = H(\underline{S}^{3i}) - H(\underline{S}^{3i} | \underline{M}^p) = 3 - 1 = 2 \text{ bits}$
- ***Can we leak less information?***

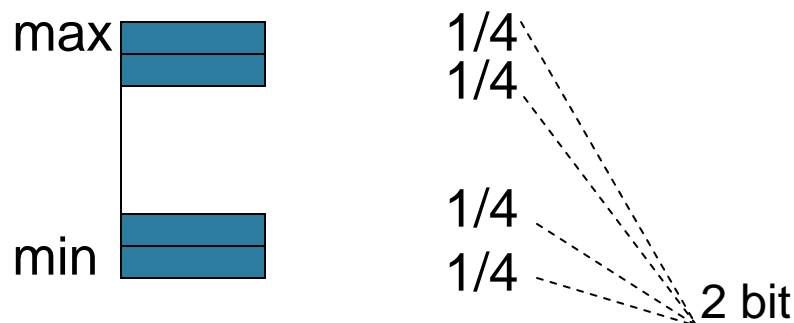
Syndrome Distribution Shaping (SDS): Intuition

IBS: pick most + or most - value, to encode a “1” bit or a “0” bit



$$LB(\underline{S}^{3i}) \equiv I(\underline{S}^{3i}; \underline{M}^\infty) = H(\underline{S}^{3i}) - H(\underline{S}^{3i} | \underline{M}^\infty) = 2 \text{ bits}$$

SDS: randomly select two max or two min



$$LB(\underline{S}^{3i}) \equiv I(\underline{S}^{3i}; \underline{M}^\infty) = H(\underline{S}^{3i}) - H(\underline{S}^{3i} | \underline{M}^\infty) = 1 \text{ bits}$$

Reduced Leaked Bits (per Syndrome Word) by “flattening” distribution

Syndrome Distribution Shaping (SDS)

Let p = probability a PUF output choice is ignored or skipped

- i.e., the max or min selection ignores that PUF output choice

Reducing Leaked Bits while preserving error correction power:

- $I(\underline{S}^{3i}, \underline{M}^\infty) = 2$ bits
- $I(\underline{S}^{W=4}, p = 1/2, \underline{M}^\infty) = 1.02$ bits
- $I(\underline{S}^{W=5}, p = 3/4, \underline{M}^\infty) = 0.80$ bits
- $I(\underline{S}^{W=6}, p = 7/8, \underline{M}^\infty) = 0.71$ bits
- $I(\underline{S}^{W=7}, p = 15/16, \underline{M}^\infty) = 0.67$ bits



“Choosing best out of 8”

“Choosing best out of 16, w/ ~half of the choices eliminated”

Leaked Bits ↓2x!

Machine Learning Results

Ruhrmair, et. al., “Modeling Attacks on PUFs”, ACM CCS 2010.

$$N_{CRP} \approx 0.5 \frac{k+1}{\varepsilon}$$

N_{CRP} : number of challenge / response pairs

k : # of delay parameters in an arbiter PUF

ε : classification error

Observation: Adversary with k C/R pairs cannot do much better than guessing, i.e., $\varepsilon \approx 0.5$.

What cannot be learned? (1)

Now rearrange the equation, rename terms, etc.

$$N_{CRP} \approx 0.5 \frac{k+1}{\varepsilon} \quad \longrightarrow \quad \varepsilon \approx \min\left(0.5 \frac{k+1}{\Sigma LB}, 0.5\right)$$

Conservative: stay safely within boundary where $\varepsilon = 0.5$ such that virtually nothing is learned from Syndrome Bits.

When $0 \leq \varepsilon < 0.5$, something is learned from the Syndrome Bits.

But how much information cannot be learned?

What cannot be learned? (2)

We know “bias” reduces min-entropy H_∞

Now, instead of “bias”, we have ε conditioned upon Syndrome Words known to the adversary at some point in time

-> Use conditional version of min-entropy

$$\tilde{H}_\infty(\underline{X} | \underline{Y}) \equiv -\log_2 (E_{y \leftarrow \underline{Y}}[2^{-H_\infty(\underline{X} | Y=y)}]) \quad [\text{Dodis, “Fuzzy Extractor”, 2004}]$$

where: $H_\infty \equiv -\log_2 (\text{pr}_{\max}(\cdot))$

we note this applies to a bit-oriented learner as well as a block-oriented learner

- What the adversary can learn is reflected in classification error ε
- \tilde{H}_∞ computes the amount of secrecy left in the system using ε
- \tilde{H}_∞ reflects the min-entropy that the ML-adversary cannot “touch” or learn

Security Sketch

1. Use Shannon unconditional security to derive LB metric

$$I(\underline{CT}^{\text{alg}}; \underline{Key}) = H(\underline{Key}) - H(\underline{Key} | \underline{CT}^{\text{alg}})$$



Can reduce using SDS

$$\text{LeakedBits}(\underline{Syn}^{\text{alg}}) = I(\underline{Syn}^{\text{alg}}; \underline{PufParam})$$



2. Assume $(\epsilon, \Sigma LB)$ -ML Adversary, e.g.,

$$\epsilon \approx \min\left(0.5 \frac{k+1}{\Sigma LB}, 0.5\right)$$

“Security-Optimized”

“PUF-Optimized”

3a. “insufficient eqs to learn system”

want $\epsilon \approx 0.5$, e.g.,

k multi-bit parameters,

$k/2$ equations w/ 1 bit outcome,

$k/2$ degrees of freedom,

secret bits $\ll k/2$

3b. “use unlearnable part of system”

ϵ reduces min-entropy (secrecy remaining) as ΣLB increase to where $\epsilon < 0.5$

$$\tilde{H}_{\infty}(\underline{X} | \underline{Y}) \equiv -\log_2 (E_{y \leftarrow \underline{Y}} [2^{-H_{\infty}(\underline{X} | \underline{Y}=y)}])$$

Now, without i.i.d. PUF output assumption...

Secure Construction #1:

- 640 OSC pairs, forming $k = 640$ “delay parameters”
- Only $k / 2$ equations (each with a 1 bit outcome) leaked via Syndrome
- 320 degrees of freedom to keep secret 128-bits of information

“insufficient equations to learn system”

Secure Construction #4:

- 128 OSC pairs, forming $k = 128$ “delay parameters”
- Use ϵ curve to compute amount of secrecy left in the system
- Can extract a 128-bit key using results from [Ruhrmair, 2010]
 - Secure against a $(\epsilon, \Sigma LB)$ Machine-Learning adversary

“use unlearnable part of system”

Conclusions

Conclusions

Lightweight PUF Key Generation

- 75% reduction in complexity from 2-stage ECC
 - Two stage ECC better characterized and also available
- Environmentally Stable
 - Temperature: -55°C to 125°C
 - Voltage: $V_{nom} \pm 10\%$
 - WC VT Corners
 - Aging: 20+ yrs @ 55°C
 - Error free, 90M+ tests, FPGA, ASIC

Implied error rate ≤ 12 parts per *billion*

Security Framework

- Security-Optimized: “Insufficient eqs to learn sys”
- PUF-Optimized: “Use unlearnable part of system”

No i.i.d. PUF output assumption

Future Work

- De-rate results to account for side channel information

THANK YOU!

Extras: PUF Randomness / Uniqueness

NIST Randomness Test Results

Verayo PUF Output bits are “random” based on NIST testing

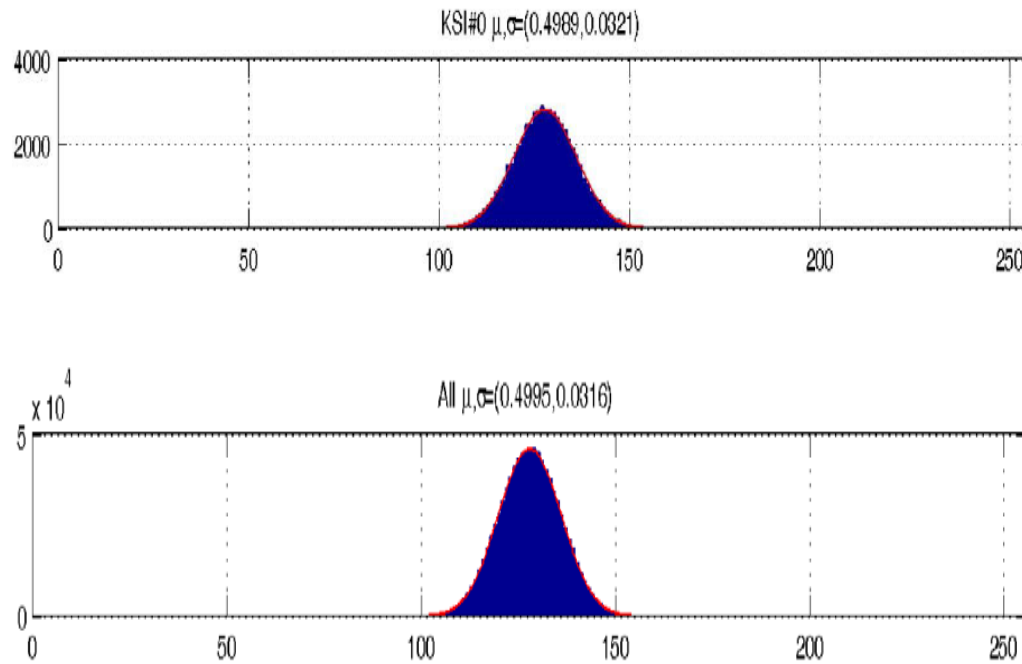
- Low bias (< +/- 1%)
- Results affirmed using on other statistical testing methods

Statistical Test	Block/Template Length	Success ratio (chip #100)	Success ratio (chip #101)	Success ratio (chip #102)	Success ratio (chip #103)	Reference bitstream ¹
Frequency	-	99%	99%	98%	99%	98%
BlockFrequency	128	100%	100%	99%	99%	97%
CumulativeSums	-	99% - 99%	99% - 100%	97% - 98%	99% - 99%	98% - 99%
Runs	-	97%	99%	100%	99%	100%
LongestRun	-	100%	100%	99%	99%	97%
Rank	-	100%	98%	100%	100%	100%
FFT	-	100%	100%	100%	100%	100%
NonOverlappingTemplate	9	94% - 100%	95% - 100%	95% - 100%	95% - 100%	95% - 100%
Overlapping Template	9	98%	98%	99%	98%	97%
Universal	-	97%	98%	100%	96%	100%
ApproximateEntropy	10	100%	99%	99%	99%	100%
RandomExcursions	-	98%-100%	97% - 100%	97% - 100%	98% - 100%	98% - 100%
RandomExcursionVariant	-	97% - 100%	97% - 100%	97% - 100%	96% - 100%	93% - 100%
Serial	16	99% - 99%	99% - 100%	99% - 100%	98% - 98%	98% - 100%
LinearComplexity	500	100%	99%	99%	99%	100%
Cumulative p-values		100% (188/188) pass	100% (188/188) pass	100% (188/188) pass	100% (188/188) pass	100% (188/188) pass
Cumulative proportions		99% (187/188) pass	99% (187/188) pass	99% (187/188) pass	99% (187/188) pass	98% (184/188) pass

¹From George Marsaglia's *Random Number CDROM*.

Uniqueness Analysis

240 PUF devices (12 FPGAs, 20 PUFs each)



Comparisons	μ	δ
57k	.1% from ideal	.0321
↓	↓	↓
920k	.05% from ideal	.0316
	↓	↓

“sample mean converges to true mean for iid process and unbiased estimator”

“Student-t distribution converges to Gaussian as sample size $\rightarrow \infty$ ”

Conclusions: μ and σ *should not get worse* with increase in number of comparisons